True Accuracy, 16-Bit ±12 V/±15 V, Serial Input Voltage Output DAC

AD5570

FEATURES

- **Full 16-bit performance**
- **1 LSB max INL and DNL**
- **Output voltage range up to ±14 V**
- **On-board reference buffers, eliminating the need for a negative reference**
- **Controlled output during power-on**
- **Temperature range of −40°C to +85°C/−40°C to +125°C**
- **Settling time of 10 µs to 0.003%**
- **Clear function to 0 V**
- **Asynchronous update of outputs ($\overline{\text{LDAC}}$ pin)**
- **Power-on reset**
- **Serial data output for daisy-chaining**
- **Data readback facility**

APPLICATIONS

- **Industrial automation**
- **Automatic test equipment**
- **Process control**
- **Data acquisition systems**
- **General-purpose instrumentation**

FUNCTIONAL BLOCK DIAGRAM

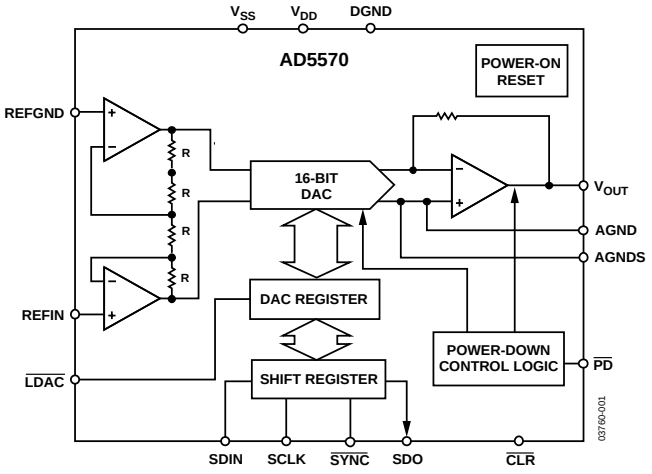

Figure 1.

GENERAL DESCRIPTION

The AD5570 is a single 16-bit serial input, voltage output DAC that operates from supply voltages of ±11.4 V up to ±16.5 V. Integral linearity (INL) and differential nonlinearity (DNL) are accurate to 1 LSB. During power-up, when the supply voltages are changing, V_{OUT} is clamped to 0 V via a low impedance path.

The AD5570 DAC comes complete with a set of reference buffers. The reference buffers allow a single, positive reference to be used. The voltage on REFIN is gained up and inverted internally to give the positive and negative reference for the DAC core. Having the reference buffers on-chip eliminates the need for external components such as inverters, precision amplifiers, and resistors, thereby reducing the overall solution size and cost.

The AD5570 uses a versatile 3-wire interface that is compatible with SPI®, QSPI™, MICROWIRE™, and DSP® interface standards. Data is presented to the part as a 16-bit serial word. Serial data is available on the SDO pin for daisy-chaining purposes. Data readback allows the user to read the contents of the DAC register via the SDO pin.

Features on the AD5570 include $\overline{\text{LDAC}}$, which can be used to update the output of the DAC. The device also has a power-down pin ($\overline{\text{PD}}$), which allows the DAC to be put into a low power state, and a $\overline{\text{CLR}}$ pin that allows the output to be cleared to 0 V.

The AD5570 is available in a 16-lead SSOP package.

PRODUCT HIGHLIGHTS

1. 1 LSB maximum INL and DNL.
2. Buffered voltage output up to ±14 V.
3. Output controlled during power-up.
4. On-board reference buffers.
5. Wide temperature range of −40°C to +125°C.

Rev. A

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REVISION HISTORY

4/05—Rev. 0 to Rev. A

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Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = +11.4 V to +16.5 V, V_{SS} = −11.4 V to −16.5 V, V_{REF} = 5 V, REFGND = AGND = DGND = 0 V, R_L = 5 kΩ and C_L = 200 pF to AGND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ[2]	Max	Unit	Test Conditions/Comments
ACCURACY					
Resolution	16			Bits	
Monotonicity	16			Bits	
Differential Nonlinearity (DNL)	−1	±0.3	+1	LSB	
Relative Accuracy (INL)					
B/Y Grade	−1	±0.4	+1	LSB	
A/W Grade	−2	±0.6	+2	LSB	
Positive INL drift over Time[3]					See Figure 16
A/B grades		2.5		ppm	
W/Y grades		6.5		ppm	
Negative Full-Scale Error		±0.9	±7.5	mV	
Full-Scale Error		±1.8	± 6	mV	
Bipolar Zero Error		±0.9	±7.5	mV	
Gain Error		±1.8	±7.5	mV	
Gain Temperature Coefficient[4]		+0.25	±1.5	ppm FSR/°C	
REFERENCE INPUT					
Reference Input Range[4]	4	5	5	V	With ±11.4 V supplies
	4	5	7	V	With ±16.5 V supplies
Input Current			±0.1	µA	
OUTPUT CHARACTERISTICS[4]					
Output Voltage Range	V_{SS} + 1.4 V		V_{DD} − 1.4 V	V	With ±11.4 V supplies
	V_{SS} + 2.5 V		V_{DD} − 2.5 V	V	With ±16.5 V supplies
Output Voltage Settling Time		12	16	µs	At 16 bits to ±0.5 LSB
		10	13	µs	To 0.0003%
		6	7	µs	512 LSB code change
Slew Rate		6.5		V/µs	Measured from 10% to 90%
Digital-to-Analog Glitch Impulse		15		nV-s	±12 V supplies; 1 LSB change around the major carry
Bandwidth		20		kHz	
Short Circuit Current		25		mA	
Output Noise Voltage Density		85		nV/Hz	f = 1 kHz; midscale loaded
DAC Output Impedance		0.35	0.5	Ω	
Digital Feedthrough		0.5		nV-s	
WARMUP TIME[5]		12		s	
LOGIC INPUTS					
Input Currents			±0.1	µA	
V_{INH}, Input High Voltage	2			V	
V_{INL}, Input Low Voltage			0.8	V	
C_{IN}, Input Capacitance		3		pF	
LOGIC OUTPUTS					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 1 mA
Floating-State Output		8		pF	

Parameter[1]	Min	Typ[2]	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}/V_{SS}	±11.4		±16.5	V	
I_{DD}		4	5	mA	V_{OUT} unloaded
I_{SS}		3.5	5	mA	V_{OUT} unloaded
Power-Down Current		16		μA	V_{OUT} unloaded
Power Supply Sensitivity[6]		0.1		LSB/V	±15 supplies ±10%; full-scale loaded
Power Dissipation		100		mW	V_{OUT} unloaded

[1] Temperature range: A and B = − 40°C to +85°C; W and Y = −40°C to +125°C.
[2] Typical specifications at ±12 V/±15 V, +25°C.
[3] These numbers are generated from the life test of the part.
[4] Guaranteed by design.
[5] Warmup time is required for the device to reach thermal equilibrium, thus achieving rated performance.
[6] Sensitivity of negative full-scale error and positive full-scale error to V_{DD}, V_{SS} variations.

STANDALONE TIMING CHARACTERISTICS

V_{DD} = +12 V ± 5%, V_{SS} = −12 V ± 5% or V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, V_{REF} = 5 V, REFGND = AGND = DGND = 0 V, R_L = 5 kΩ, and C_L = 200 pF to AGND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter [1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MAX}	10	MHz max	SCLK frequency
t_1	100	ns min	SCLK cycle time
t_2	35	ns min	SCLK high time
t_3	35	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	35	ns min	Data setup time
t_6	0	ns min	Data hold time
t_7	45	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	45	ns min	Minimum $\overline{SYNC}$ high time
t_9	0	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{10}	50	ns min	$\overline{LDAC}$ pulse width
t_{11}	0	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge (no update)
t_{12}	0	ns min	$\overline{LDAC}$ rising edge to $\overline{SYNC}$ rising edge (no update)
t_{13}	20	ns min	$\overline{CLR}$ pulse width

[1] All parameters guaranteed by design and characterization. Not production tested.
[2] All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} +V_{IH})/2.

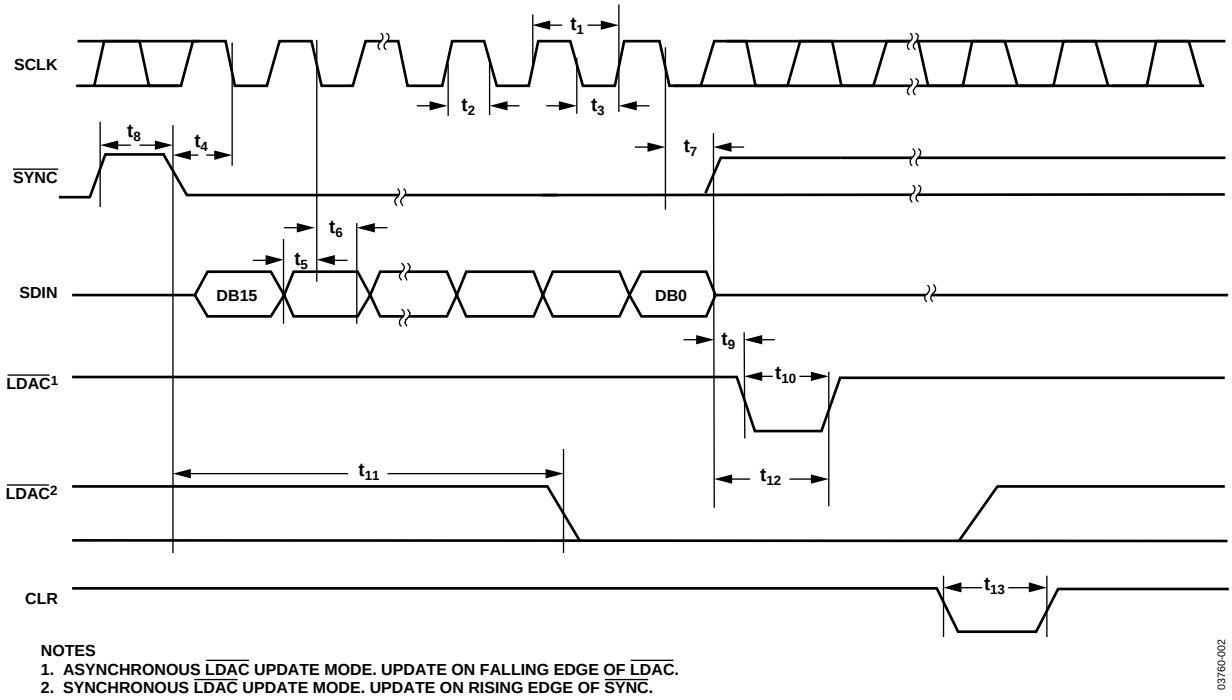

Figure 2. Serial Interface Timing Diagram

DAISY-CHAINING AND READBACK TIMING CHARACTERISTICS

V_{DD} = +12 V ± 5%, V_{SS} = −12 V ± 5% or V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%; V_{REF} = 5 V; REFGND = AGND = DGND = 0 V; R_L = 5 kΩ, and C_L = 200 pF to AGND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MAX}	2	MHz max	SCLK frequency
t_1	500	ns min	SCLK cycle time
t_2	200	ns min	SCLK high time
t_3	200	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	35	ns min	Data setup time
t_6	0	ns min	Data hold time
t_7	45	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	45	ns min	Minimum $\overline{SYNC}$ high time
t_9	0	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{10}	50	ns min	$\overline{LDAC}$ pulse width
t_{14}[3]	200	ns max	Data delay on SDO

[1] All parameters guaranteed by design and characterization. Not production tested.
[2] All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} +V_{IH})/2. SDO; R_{PULLUP} = 5 kΩ, C_L = 15 pF.
[3] With C_L = 0 pF, t_{15} = 100 ns.

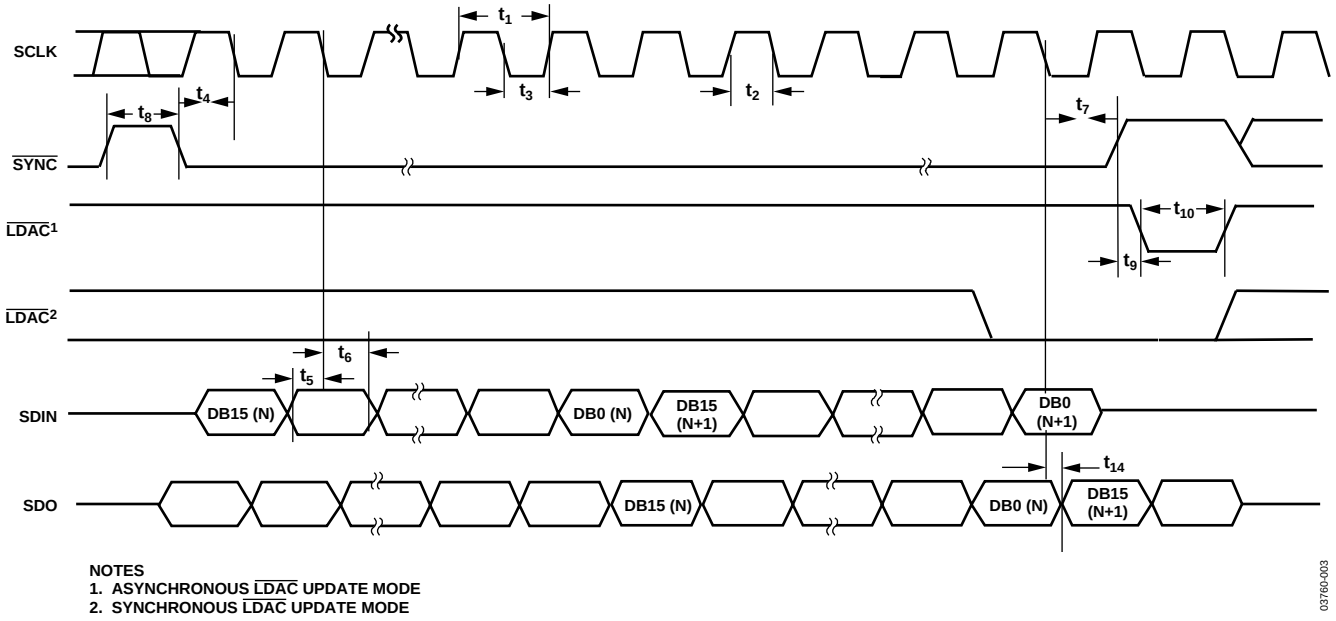

Figure 3. Daisy-Chaining Timing Diagram

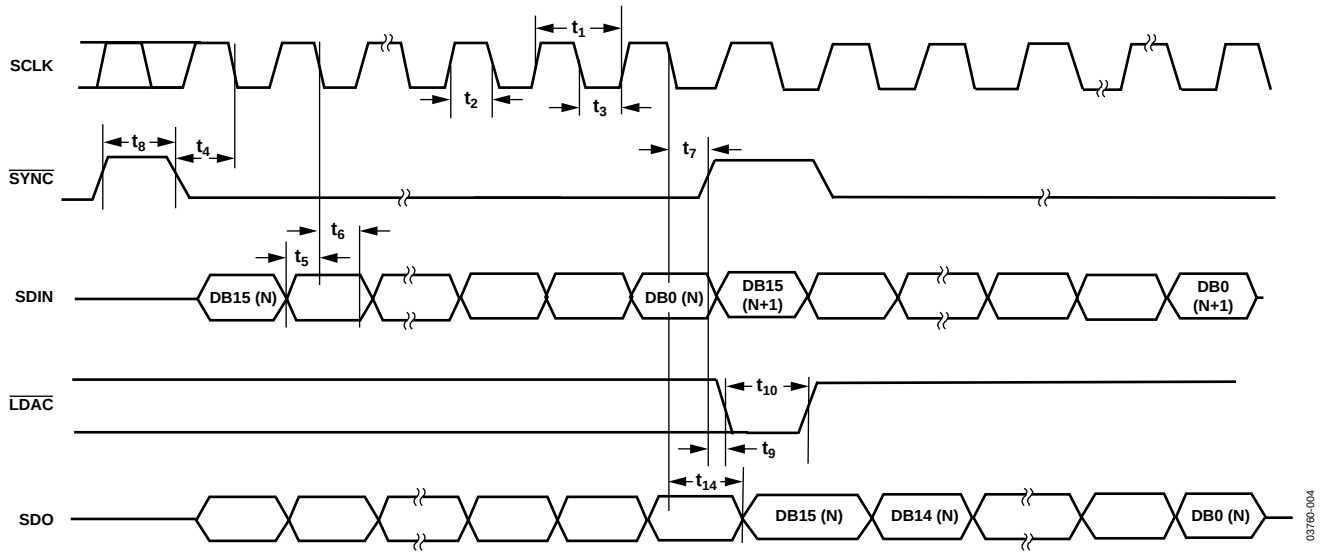

Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND, AGNDS, DGND	−0.3 V, +17 V
V_{SS} to AGND, AGNDS, DGND	+0.3 V, −17 V
AGND, AGNDS to DGND	−0.3 V to +0.3 V
REFGND to AGND, ADNDS	−0.3 V to + 0.3 V
REFIN to AGND, AGNDS	−0.3 V to +17 V
REFIN to REFGND	−0.3 V to +17 V
Digital Inputs to DGND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND, AGNDS	V_{SS} − 0.3 V to V_{DD} + 0.3 V
SDO to DGND	−0.3 V to +6.5 V
Operating Temperature Range	
W, Y Grades	−40°C to +125°C
A, B Grades	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	
(T_J max)	150°C
16-Lead SSOP Package	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	139°C/W
Lead Temperature (Soldering 10 sec)	300°C
IR Reflow, Peak Temperature	230°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

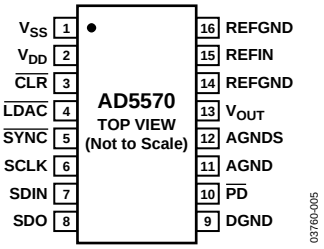

Figure 5. 16-Lead SSOP Pin Configuration (RS-16)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{SS}	Negative Analog Supply Voltage. −12 V ± 5% to −15 V ± 10% for specified performance.
2	V_{DD}	Positive Analog Supply Voltage. 12 V ± 5% to 15 V ± 10% for specified performance.
3	$\overline{CLR}$	Level Sensitive, Active Low Input. A falling edge of $\overline{CLR}$ resets V_{OUT} to AGND. The contents of the registers are untouched.
4	$\overline{LDAC}$	Active Low Control Input. Transfers the contents of the input register to the DAC register. $\overline{LDAC}$ can be tied permanently low, enabling the outputs to be updated on the rising edge of $\overline{SYNC}$.
5	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the data. When $\overline{SYNC}$ goes low, it powers on the SCLK and SDIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 16 clocks.
6	SCLK	Serial Clock Input. Data is clocked into the input register on the falling edge of the serial clock input. Data can be transferred at rates of up to 8 MHz.
7	SDIN	Serial Data Input. This device has a 16-bit register. Data is clocked into the register on the falling edge of the serial clock input.
8	SDO	Serial Data Output. Can be used for daisy-chaining a number of devices together or for reading back the data in the shift register for diagnostic purposes. This is an open-drain output; it should be pulled to logic high with an external pull-up resistor of ~5 kΩ.
9	DGND	Digital Ground. Ground reference for all digital circuitry.
10	$\overline{PD}$	Active Low Control Input. Allows the DAC to be put into a power-down state.
11	AGND	Analog Ground. Ground reference for all analog circuitry.
12	AGNDS	Analog Ground Sense. This is normally tied to AGND.
13	V_{OUT}	Analog Output Voltage.
14, 16	REFGND	Reference Ground. This pin should be tied to 0 V.
15	REFIN	Voltage Reference Input. This is internally buffered before being applied to the DAC. For bipolar ±10 V output range, REFIN is 5 V.

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
Relative accuracy or integral nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital inputs. The AD5570 is monotonic over its full operating temperature range.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from the ideal.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Negative Full-Scale Error/Zero Scale Error
Negative full-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC latch. Ideally, the output voltage, with all 0s in the DAC latch, should be $-2\ V_{REF}$.

Full-Scale Error
Full-scale error is the error in the DAC output voltage when all 1s are loaded to the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch should be $2\ V_{REF} - 1$ LSB.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog input from the ideal half-scale output of 0.0000 V when the inputs are loaded with 0x8000.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of output voltage. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the amount of charge injected into the analog output when the input codes in the DAC register change state. It is specified as the area of the glitch in nV-s and is measured when the digital input code changes by 1 LSB at the major carry transition, that is, from code 0x7FFF to 0x8000.

Bandwidth
The reference amplifiers within the DAC have a finite bandwidth to optimize noise performance. To measure it, a sine wave is applied to the reference input (REFIN), with full-scale code loaded to the DAC. The bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{\text{SYNC}}$ is held high, while the SCLK and SDIN signals are toggled. Digital feedthrough is specified in nV-s and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

Power Supply Sensitivity
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

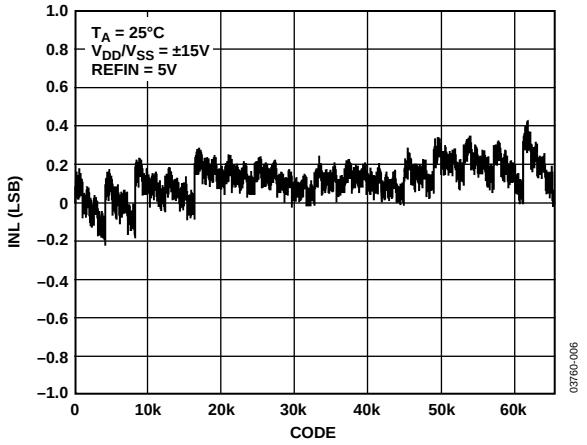

Figure 6. Integral Nonlinearity vs. Code, V_{DD}/V_{SS} = ±15 V

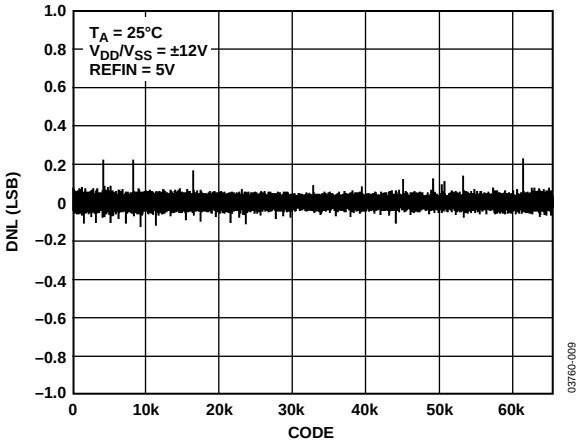

Figure 9. Differential Nonlinearity vs. Code, V_{DD}/V_{SS} = ±12 V

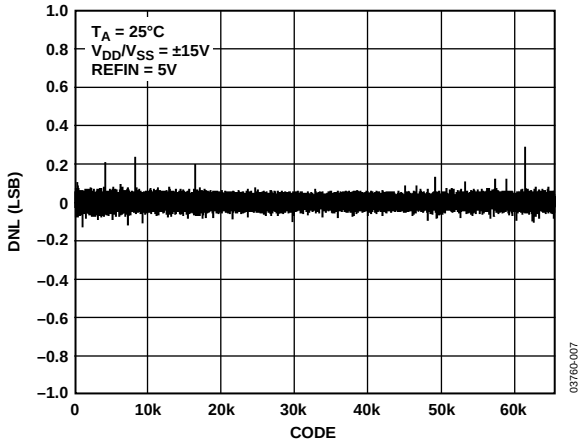

Figure 7. Differential Nonlinearity vs. Code, V_{DD}/V_{SS} = ±15 V

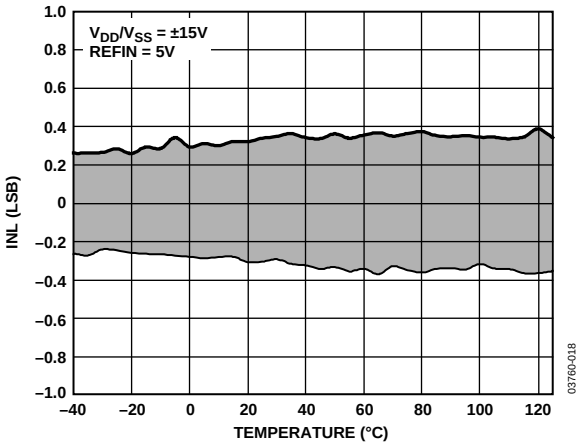

Figure 10. Integral Nonlinearity vs. Temperature, ±15 V Supplies

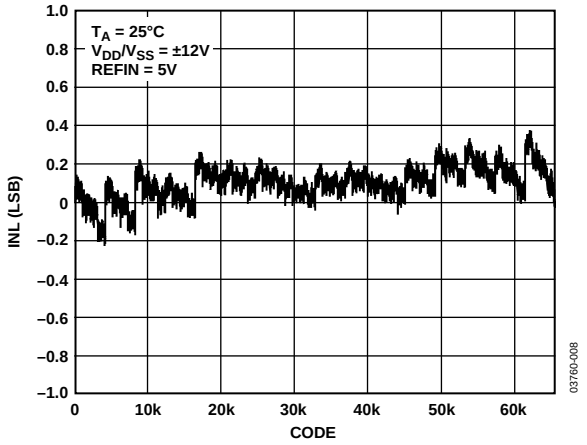

Figure 8. Integral Nonlinearity vs. Code, V_{DD}/V_{SS} = ±12 V

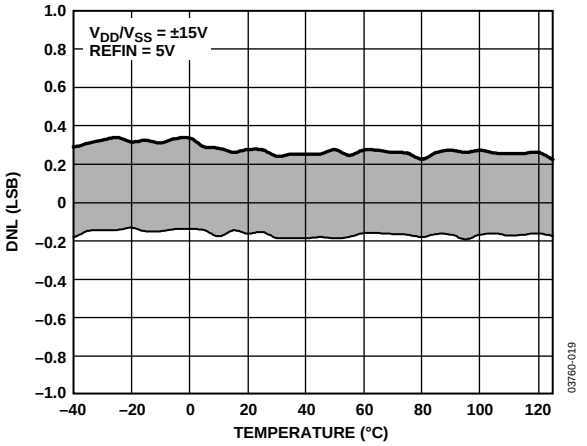

Figure 11. Differential Nonlinearity vs. Temperature, ±15 V Supplies

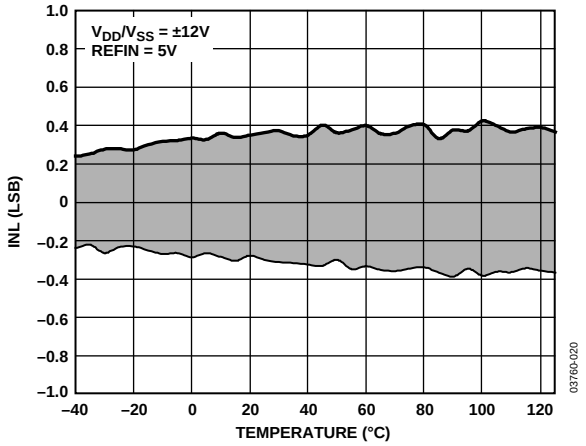

Figure 12. Integral Nonlinearity vs. Temperature, ±12 V Supplies

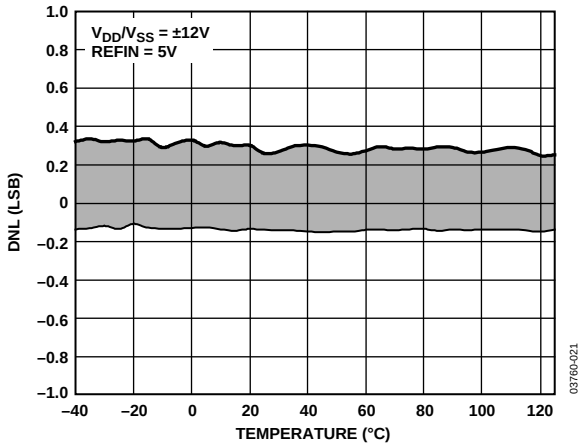

Figure 13. Differential Nonlinearity vs. Temperature, ±12 V Supplies

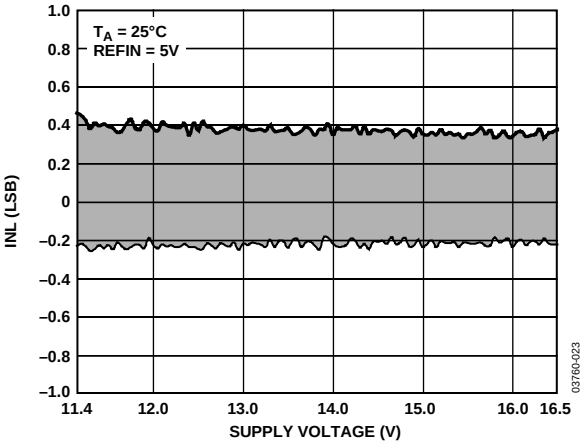

Figure 14. Integral Nonlinearity vs. Supply Voltage

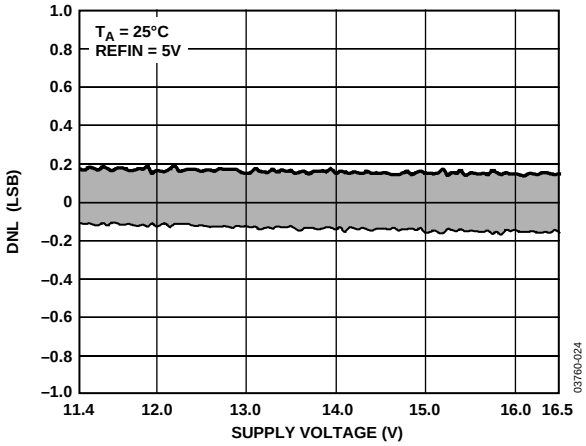

Figure 15. Differential Nonlinearity vs. Supply Voltage

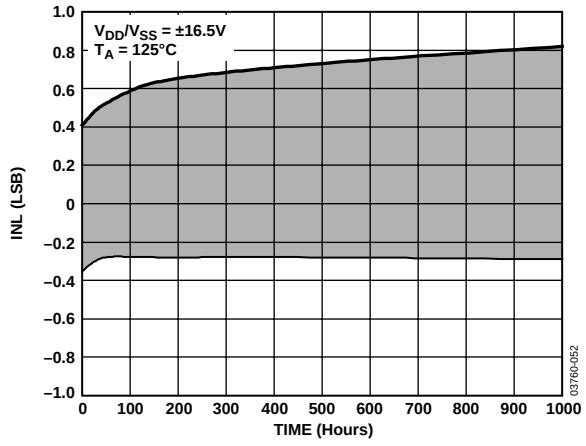

Figure 16. INL Drift over Time

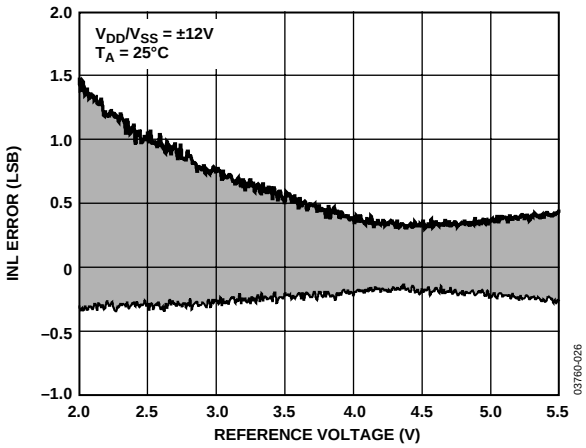

Figure 17. Integral Nonlinearity Error vs. Reference Voltage, ±12 V Supplies

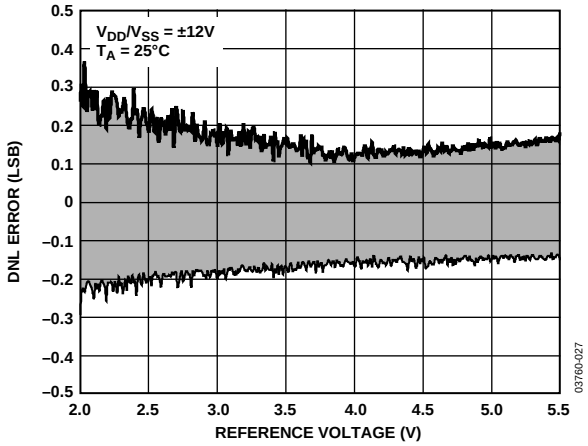

Figure 18. Differential Nonlinearity Error vs. Reference Voltage, ±12 V Supplies

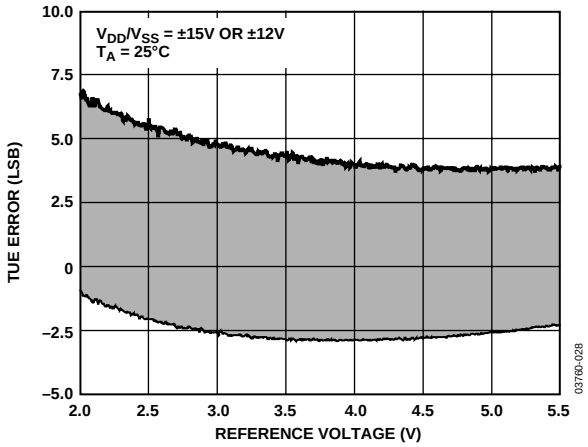

Figure 19. TUE Error vs. Reference Voltage

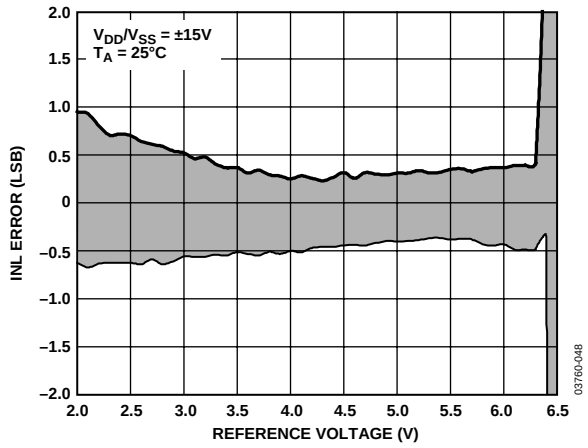

Figure 20. Integral Nonlinearity Error vs. Reference Voltage, ±15 V Supplies

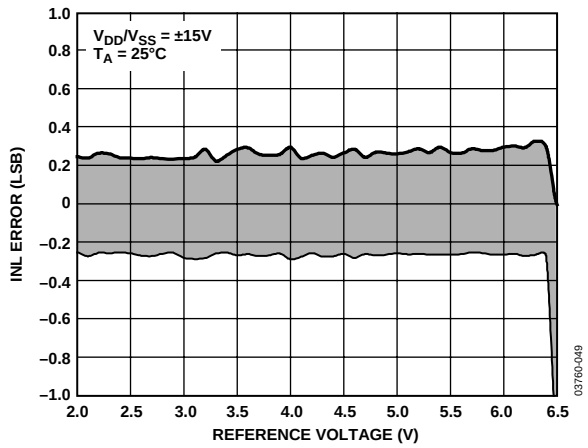

Figure 21. Differential Nonlinearity Error vs. Reference Voltage, ±15 V Supplies

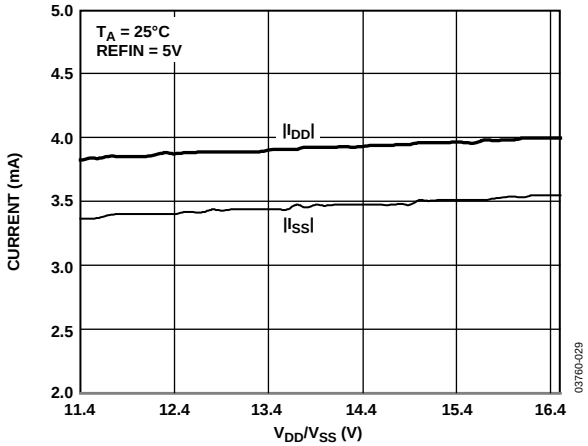

Figure 22. I_{DD}/I_{SS} vs.V_{DD}/V_{SS}

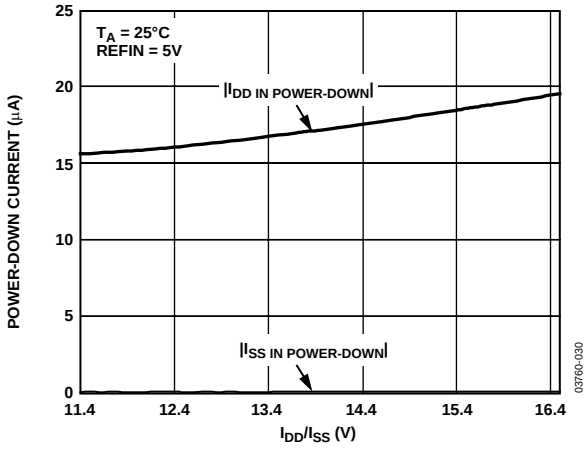

Figure 23. I_{DD}/I_{SS} in Power-Down vs. Supply Voltage

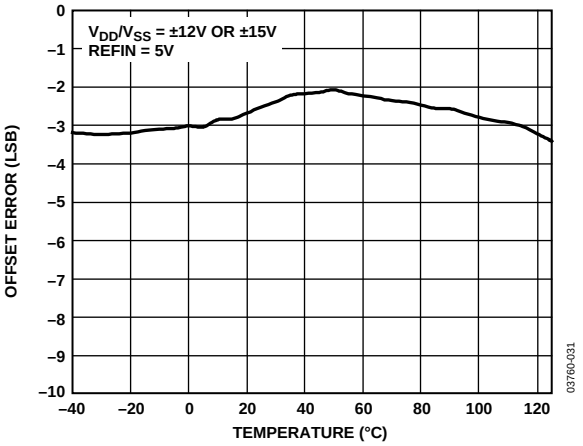

Figure 24. Offset Error vs. Temperature

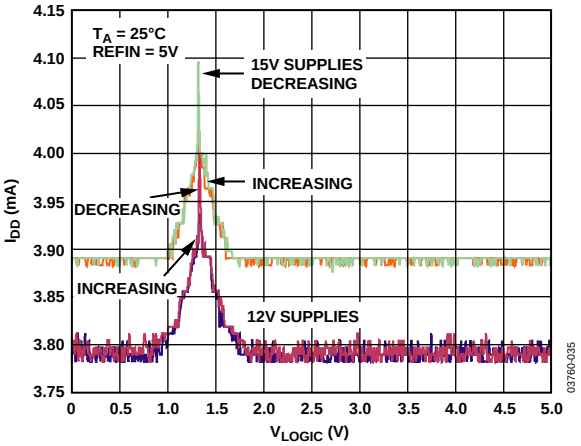

Figure 27. Supply Current vs. Logic Input Current for SCLK, $\overline{SYNC}$, SDIN, and $\overline{LDAC}$ Increasing and Decreasing

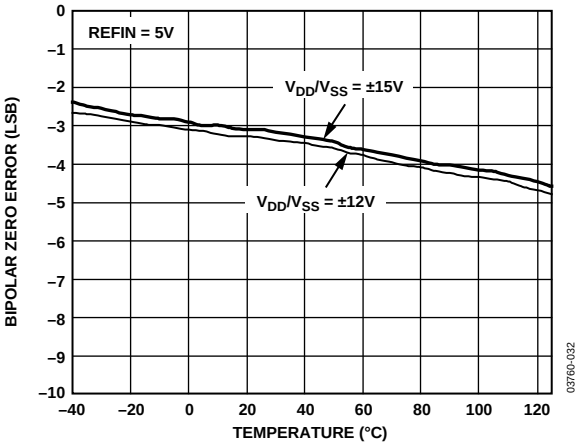

Figure 25. Bipolar Zero Error vs. Temperature

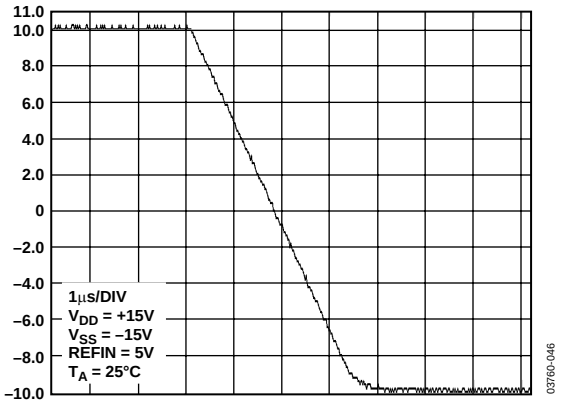

Figure 28. Settling Time

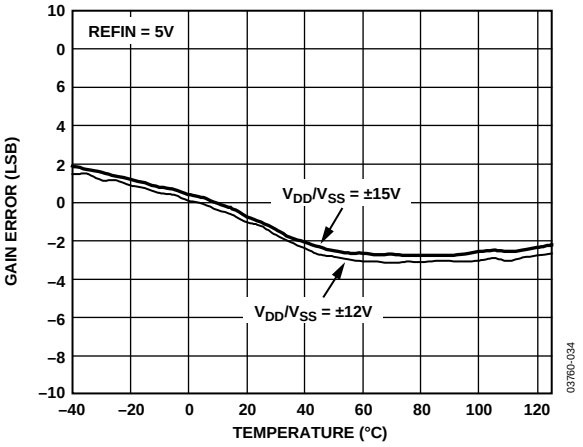

Figure 26. Gain Error vs. Temperature

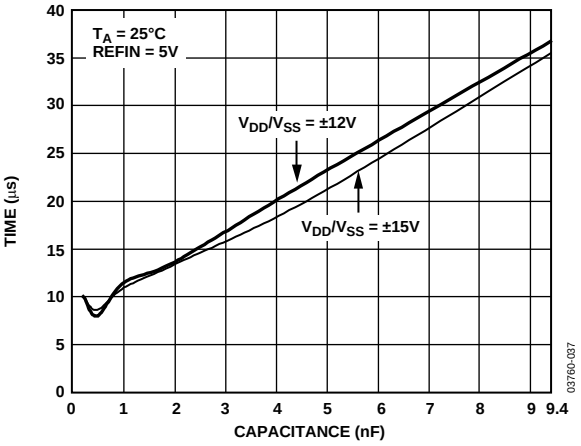

Figure 29.14-Bit Settling Time vs. Load Capacitance

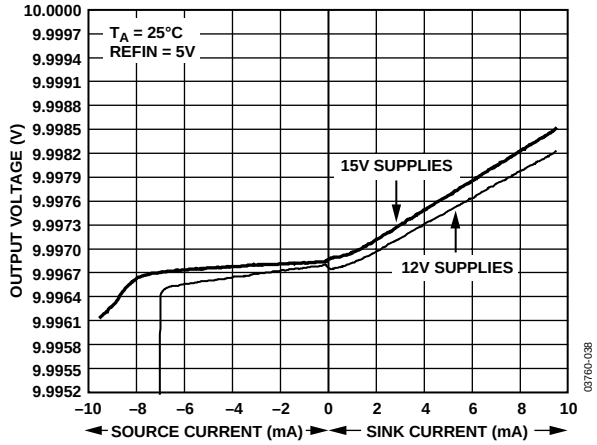

Figure 30. Source and Sink Capability of Output Amplifier with Full-Scale Loaded

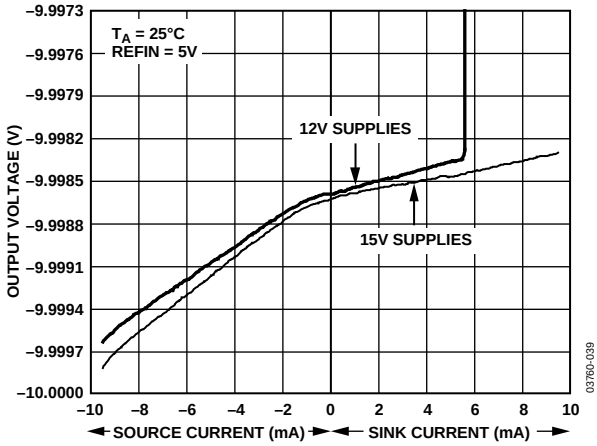

Figure 31. Source and Sink Capability of Output Amplifier with Zero-Scale Loaded

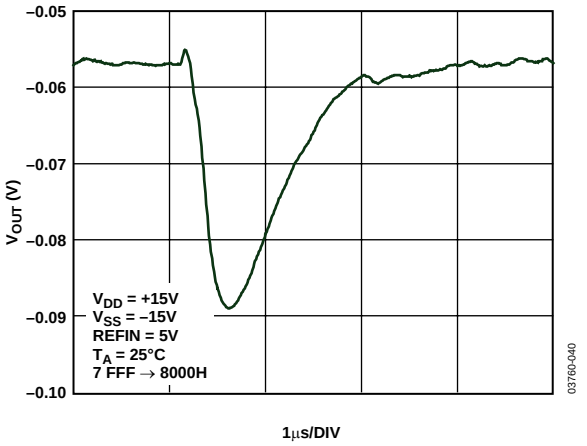

Figure 32. Major Code Transition Glitch Energy, ±15 V Supplies

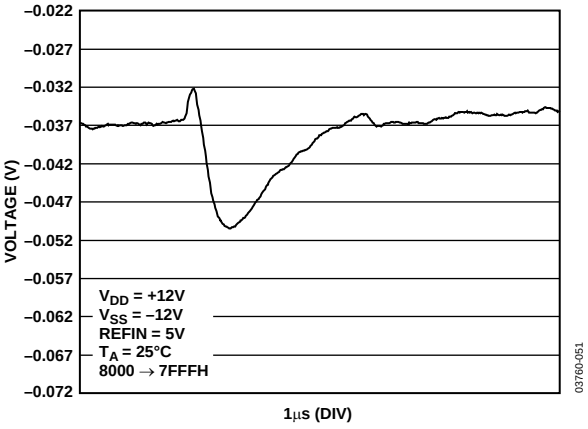

Figure 33. Major Code Transition Glitch Energy, ±12 V Supplies

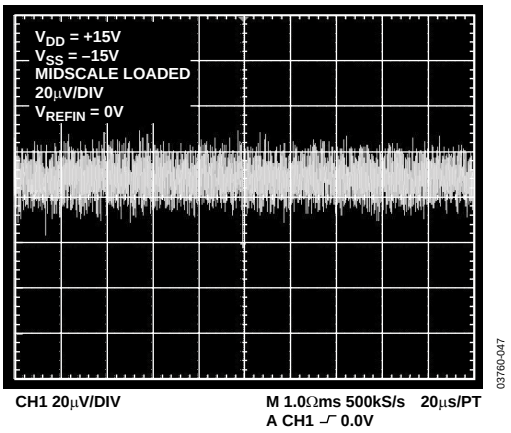

Figure 34. Peak-to-Peak Noise (100 kHz Bandwidth)

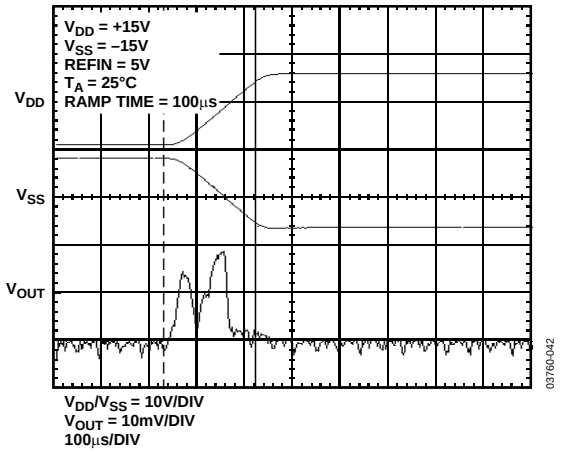

Figure 35. V_{OUT} vs. V_{DD}/V_{SS} on Power-Up

GENERAL DESCRIPTION

The AD5570 is a single 16-bit serial input, voltage output DAC. It operates from supply voltages of ±11.4 V to ±16.5 V, and has a buffered voltage output of up to ±13.6 V. Data is written to the AD5570 in a 16-bit word format, via a 3-wire serial interface. The device also offers an SDO pin, which is available for daisy-chaining or readback.

The AD5570 incorporates a power-on reset circuit, which ensures the DAC output powers up to 0 V. The device also has a power-down pin, which reduces the typical current consumption to 16 μA.

DAC ARCHITECTURE

The DAC architecture of the AD5570 consists of a 16-bit current-mode segmented R-2R DAC. The simplified circuit diagram for the DAC section is shown in Figure 36.

The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGND or IOUT. The remaining 12 bits of the data word drive switches S0 to S11 of the 12-bit R-2R ladder network.

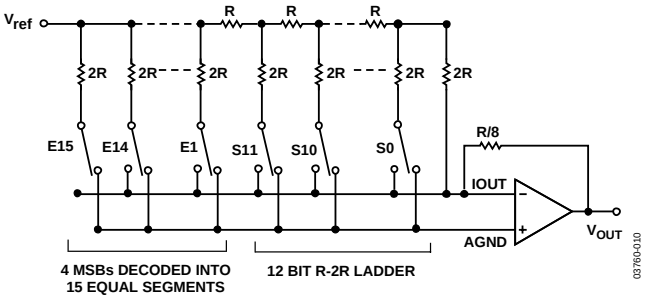

Figure 36. DAC Ladder Structure

REFERENCE BUFFERS

The AD5570 operates with an external reference. The reference input (REFIN) has an input range of up to 7 V. This input voltage is then used to provide a buffered positive and negative reference for the DAC core. The positive reference is given by

$$+V_{REF} = 2 \times V_{REFIN}$$

while the negative reference to the DAC core is given by

$$-V_{REF} = 2 \times V_{REFIN}$$

These positive and negative reference voltages define the DAC output range.

SERIAL INTERFACE

The AD5570 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 10 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 2.

On power-up, the input shift register and DAC register are loaded with midscale (0x8000). The DAC coding is straight binary; all 0s produce an output of $-2\ V_{REF}$; all 1s produce an output of $+2\ V_{REF} - 1$ LSB.

The $\overline{\text{SYNC}}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. $\overline{\text{SYNC}}$ must frame the serial word being loaded into the device. Data can be transferred into the device only while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low, observing the minimum $\overline{\text{SYNC}}$ to SCLK falling edge setup time, t_4. After $\overline{\text{SYNC}}$ goes low, serial data on SDIN is shifted into the device's input shift register on the falling edges of SCLK. $\overline{\text{SYNC}}$ can be taken high after the falling edge of the 16th SCLK pulse, observing the minimum SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time, t_7.

After the end of the serial data transfer, data is automatically transferred from the input shift register to the input register of the DAC.

When data has been transferred into the input register of the DAC, the DAC register and DAC output can be updated by taking $\overline{\text{LDAC}}$ low while $\overline{\text{SYNC}}$ is high.

Load DAC Input ($\overline{\text{LDAC}}$)

There are two ways in which the DAC register and DAC output can be updated when data has been transferred into the input register of the DAC. Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, one of two update modes is selected.

The first mode is synchronous $\overline{\text{LDAC}}$. In this mode, $\overline{\text{LDAC}}$ is low while data is being clocked into the input shift register. The DAC output is updated when $\overline{\text{SYNC}}$ is taken high. The update here occurs on the rising edge of $\overline{\text{SYNC}}$.

The second mode is asynchronous $\overline{\text{LDAC}}$. In this mode, $\overline{\text{LDAC}}$ is high while data is being clocked in. The DAC output is updated by taking $\overline{\text{LDAC}}$ low any time after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

Figure 37 shows a simplified block diagram of the input loading circuitry.

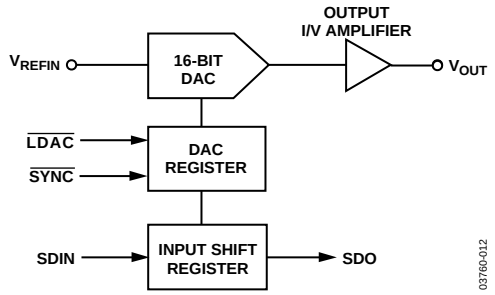

Figure 37. Simplified Serial Interface Showing Input Loading Circuitry

TRANSFER FUNCTION

Table 6 shows the ideal input code to output voltage relationship for the AD5570.

Table 6. Binary Code Table

Digital Input				
MSB			**LSB**	**Analog Output—V_{OUT}**
1111	1111	1111	1111	+2 V_{REF} × (32,767/32,768)
1000	0000	0000	0001	+2 V_{REF} × (1/32,768)
1000	0000	0000	0000	0 V
0111	1111	1111	1111	−2 V_{REF} × (1/32,768)
0000	0000	0000	0000	−2 V_{REF}

The output voltage expression is given by

$$V_{OUT} = -2V_{REFIN} + 4 \times V_{REFIN}[D/65536]$$

where:
D is the decimal equivalent of the code loaded to the DAC.
V_{REFIN} is the reference voltage available at the REFIN pin.

CLEAR ($\overline{\text{CLR}}$)

$\overline{\text{CLR}}$ is an active low digital input that allows the output to be cleared to 0 V. When the $\overline{\text{CLR}}$ signal is brought back high, the output stays at 0 V until $\overline{\text{LDAC}}$ is brought low. The relationship between $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ is explained further in Table 7.

Table 7. Relationships Among $\overline{\text{PD}}$, $\overline{\text{CLR}}$, and $\overline{\text{LDAC}}$

$\overline{\text{PD}}$	$\overline{\text{CLR}}$	$\overline{\text{LDAC}}$	Comments
0	x	x	$\overline{\text{PD}}$ has priority over $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$. The output remains at 0 V through an internal 20 kΩ resistor. It is still possible to address both the input register and DAC register when the AD5570 is in power-down.
1	0	0	Data is written to the input register and DAC register. $\overline{\text{CLR}}$ has higher priority over $\overline{\text{LDAC}}$; therefore, the output is at 0 V.
1	0	1	Data is written to the input register only. The output is at 0 V and remains at 0 V, when $\overline{\text{CLR}}$ is taken back high.
1	1	0	Data is written to the input register and the DAC register. The output is driven to the DAC level.
1	1	1	Data is written to the input register only. The output of the DAC register is unchanged.

POWER-DOWN ($\overline{\text{PD}}$)

The power-down pin allows the user to place the AD5570 into a power-down mode. In power-down mode, power consumption is at a minimum; the device typically consumes only 16 µA.

POWER-ON RESET

The AD5570 contains a power-on reset circuit that controls the output during power-up and power-down. This is useful in applications where the known state of the output of the DAC during power-up is important. On power-up and power-down, the output of the DAC, V_{OUT}, is held at AGND.

SERIAL DATA OUTPUT (SDO)

The SDO is the internal shift register's output. For the AD5570, SDO is an internal pull-down only; an external pull-up resistor of ~5 kΩ to external logic high is required. SDO pull-down is disabled when the device is in power-down, thus saving current.

The availability of SDO allows any number of AD5570s to be daisy-chained together. It also allows for the contents of the DAC register, or any number of DACs daisy-chained together, to be read back for diagnostic purposes.

Daisy Chaining

This mode of operation is designed for multi-DAC systems, where several AD5570s can be connected in cascade as shown in Figure 38. This is done by connecting the control inputs in parallel and then daisy-chaining the SDIN and SDO I/Os of each device. An external pull-up resistor of ~5 kΩ on SDO is required when using the part in daisy-chain mode.

As described earlier, when $\overline{\text{SYNC}}$ goes low, serial data on SDIN is shifted into the input shift register on the falling edge of SCLK. If more than 16 clock pulses are applied, the data ripples out of the shift resister and appears on the SDO line. By connecting this line to the SDIN input on the next AD5570 in the chain, a multi-DAC interface can be constructed.

One data transfer cycle of 16 SCLK pulses is required for each DAC in the system. Therefore, the total number of clock cycles must equal 16 N, where N is the total number of devices in the chain. The first data transfer cycle written into the chain appears at the last DAC in the system on the final data transfer cycle.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This prevents any further data from being clocked into the devices.

A continuous SCLK source can be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles can be used and $\overline{\text{SYNC}}$ taken high some time later. The outputs of all the DACs in the system can be updated simultaneously using the $\overline{\text{LDAC}}$ signal.

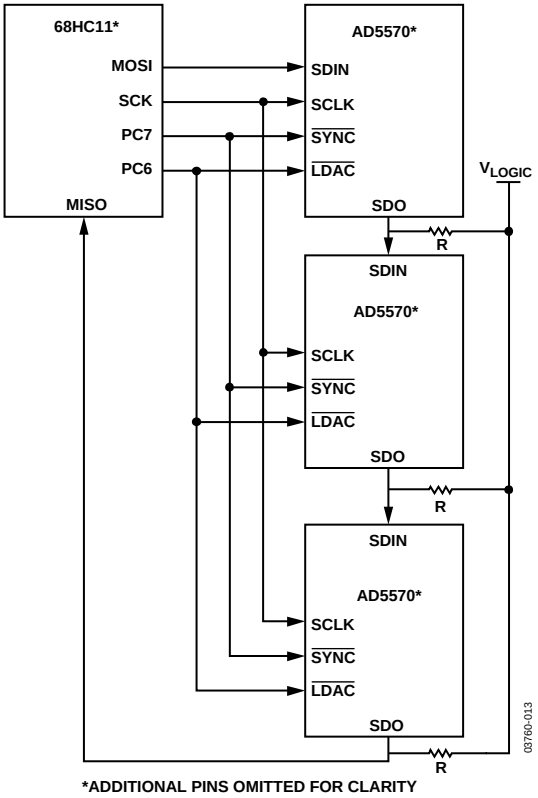

Figure 38. Daisy Chaining Using the AD5570

Readback

The AD5570 allows the data contained in the DAC register to be read back, if required. As with daisy chaining, an external pull-up resistor of ~5 kΩ on SDO is required. The data in the DAC register is available on SDO on the falling edges of SCLK when $\overline{\text{SYNC}}$ is low. On the 16th SCLK edge, SDO is updated to repeat SDIN with a delay of 16 clock cycles.

To read back the contents of the DAC register without writing to the part, $\overline{\text{SYNC}}$ should be taken low while $\overline{\text{LDAC}}$ is held high.

Daisy-chaining readback is also possible through the SDO pin of the last device in the DAC chain, because the DAC data passes through the DAC chain with the appropriate latency.

APPLICATIONS INFORMATION

TYPICAL OPERATING CIRCUIT

Figure 39 shows the typical operating circuit for the AD5570. The only external component needed for this precision 16-bit DAC is a single external positive reference. Because the device incorporates reference buffers, it eliminates the need for a negative reference, external inverters, precision amplifiers, and resistors. This leads to an overall savings of both cost and board space.

In the circuit shown in Figure 39, V_{DD} and V_{SS} are both connected to ±15 V, but V_{DD} and V_{SS} can operate supplies from +11.4 V to +16.5 V. In Figure 39, AGNDS is connected to AGND, but the option of Force/Sense is included on this device, if required by the user.

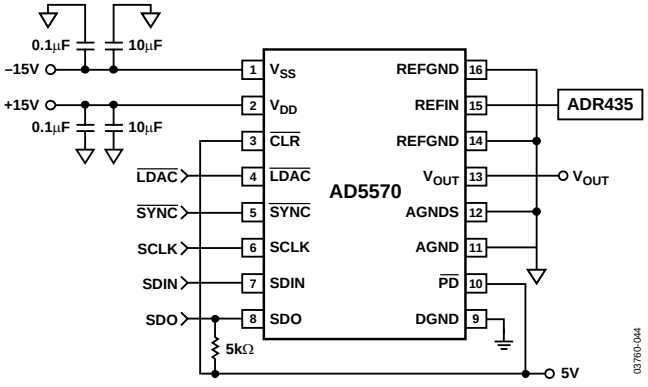

Figure 39. Typical Operating Circuit

Force/Sense of AGND

Because of the extremely high accuracy of this device, system design issues, such as grounding and contact resistance, are very important. The AD5570, with ±10 V output, has an LSB size of 305 µV. Therefore, series wiring and connector resistances of very small values can cause voltage drops of an LSB. For this reason, the AD5570 offers a Force/Sense output configuration.

Figure 40 shows how to connect the AD5570 to the Force/Sense amplifier. Where accuracy of the output is important, an amplifier such as the OP177 is ideal. The OP177 is ultraprecise with offset voltages of 10 µV maximum at room temperature, and offset drift of 0.1 µV/°C maximum. Alternative recommended amplifiers are the OP1177 and the OP77. For applications where optimization of the circuit for settling time is needed, the AD845 is recommended.

Precision Voltage Reference Selection

To achieve the optimum performance from the AD5570, thought should be given to the selection of a precision voltage reference. The AD5570 has just one reference input, REFIN. This voltage on REFIN is used to provide a buffered positive and negative reference for the DAC core. Therefore, any error in the voltage reference is reflected in the output of the device.

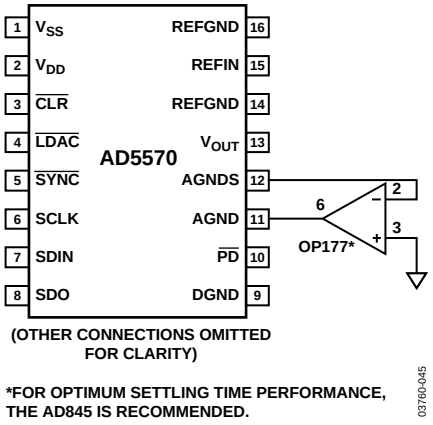

Figure 40. Driving AGND and AGNDS Using a Force/Sense Amplifier

The four possible sources of error to consider when choosing a voltage reference for high accuracy applications are initial accuracy, temperature coefficient of the output voltage, long-term drift, and output voltage noise.

Initial accuracy on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy specification is preferred. Also, choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim out system errors by setting the reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift (LTD) is a measure of how much the reference drifts over time. A reference with a tight long-term drift specification ensures the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. It is important to choose a reference with as low an output noise voltage as practical for the system resolution required. Precision voltage references, such as the ADR435 (XFET® design), produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference can be required to minimize the output noise.

Table 8. Partial List of Precision References Recommended for Use with the AD5570

Part No.	Initial Accuracy (mV max)	Long-Term Drift (ppm typ)	Temp Drift (ppm/°C max)	0.1 Hz to 10 Hz Noise (μV p-p typ)
ADR435	± 6	30	3	3.4
ADR425	± 6	50	3	3.4
ADR02[1]	±5	50	3	15
ADR395	±6	50	25	5
AD586	±2.5	15	10	4

[1]Available in SC70 package.

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5570 is mounted should be designed so the analog and digital sections are separated and confined to certain areas of the board. If the AD5570 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5570 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5570 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines reduces crosstalk between them; this is not required on a multilayer board, which has a separate ground plane, but separating the lines helps. It is essential to minimize noise on the REFIN line, because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

OPTO-ISOLATORS

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators provide voltage isolation in excess of 3 kV. The serial loading structure of the AD5570 makes it ideal for opto-isolated interfaces, because the number of interface lines is kept to a minimum. Figure 41 shows a 4-channel isolated interface to the AD5570. To reduce the number of opto-isolators, the $\overline{\text{LDAC}}$ pin can be tied permanently low if the simultaneous updating of the DAC is not required. The DAC can then be updated on the rising edge of $\overline{\text{SYNC}}$.

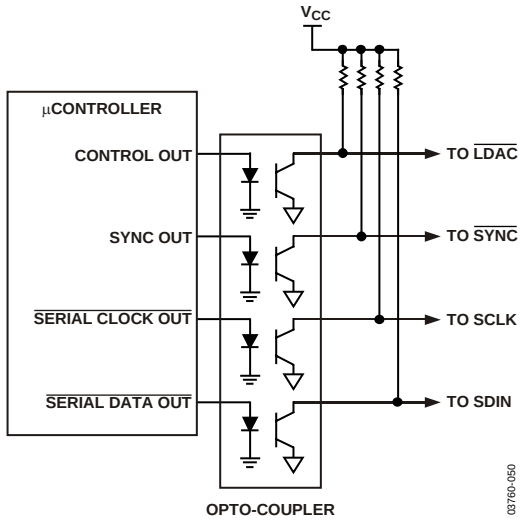

Figure 41. Opto-Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5570 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5570 requires a 16-bit data word with data valid on the falling edge of SCLK.

For all the interfaces, the DAC output update can be done automatically when all the data is clocked in, or it can be done under the control of $\overline{\text{LDAC}}$. The contents of the DAC register can be read using the readback function.

AD5570 to MC68HC11 Interface

Figure 42 shows an example of a serial interface between the AD5570 and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), clock polarity bit (CPOL = 0), and the clock phase bit (CPHA = 1). The SPI is configured by writing to the SPI control register (SPCR); see the *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5570, the MOSI output drives the serial data line (DIN) of the AD5570, and the MISO input is driven from SDO. The $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case, PC7.

When data is being transmitted to the AD5570, the $\overline{\text{SYNC}}$ line (PC7) is taken low and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK. Eight falling clock edges occur in the transmit cycle; therefore, in order to load the required 16-bit word, PC7 is not brought high until the second 8-bit word has been transferred to the DAC's input shift register.

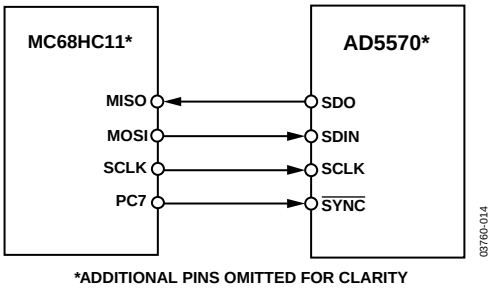

Figure 42. AD5570 to MC68HC11 Interface

$\overline{\text{LDAC}}$ is controlled by the PC6 port output. The DAC can be updated after each 2-byte transfer by bringing $\overline{\text{LDAC}}$ low. This example does not show other serial lines for the DAC. If $\overline{\text{CLR}}$ were used, it could be controlled by port output PC5, for example.

AD5570 to 8051 Interface

The AD5570 requires a clock synchronized to the serial data. For this reason, the 8051 must be operated in Mode 0. In this mode, serial data enters and exits through RxD, and a shift clock is output on RxD.

P3.3 and P3.4 are bit-programmable pins on the serial port and are used to drive $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, respectively.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user must ensure that the data in the SBUF register is arranged correctly, because the DAC expects MSB first.

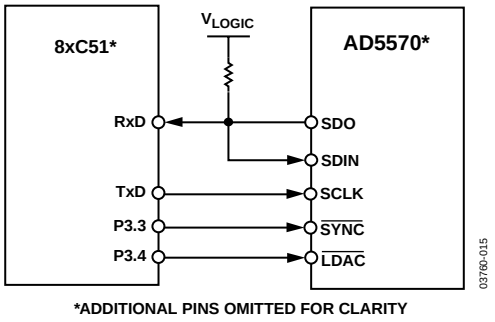

Figure 43. AD5570 to 8051 Interface

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge. As a result, no glue logic is required between this DAC and the microcontroller interface.

The 8051 transmits data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Because the DAC expects a 16-bit word, $\overline{\text{SYNC}}$ (P3.3) must be left low after the first eight bits are transferred. After the second byte has been transferred, the P3.3 line is taken high. The DAC can be updated using $\overline{\text{LDAC}}$ via P3.4 of the 8051.

AD5570 to ADSP2101/ADSP2103

An interface between the AD5570 and the ADSP2101/ADSP2103 is shown in Figure 44. The ADSP2101/ADSP2103 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP2101/ADSP2103 are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length.

Transmission is initiated by writing a word to the Tx register, after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the DAC. In the interface shown, the DAC output is updated using the $\overline{\text{LDAC}}$ pin via the DSP. Alternatively, the $\overline{\text{LDAC}}$ input can be tied permanently low, and then the update is automatic when $\overline{\text{TFS}}$ is taken high.

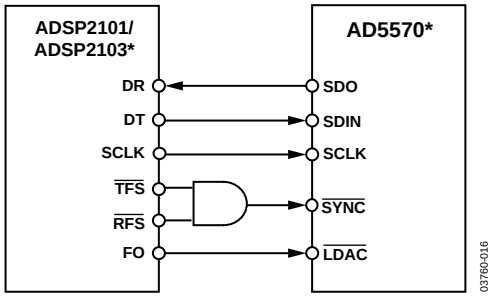

Figure 44. AD5570 to ADSP2101/ADSP2103 Interface

AD5570 to PIC16C6x/7x

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit set to 0. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual.* In this example, I/O port RA1 is being used to pulse $\overline{\text{SYNC}}$ and enable the serial port of the AD5570. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are needed. Figure 45 shows the connection diagram.

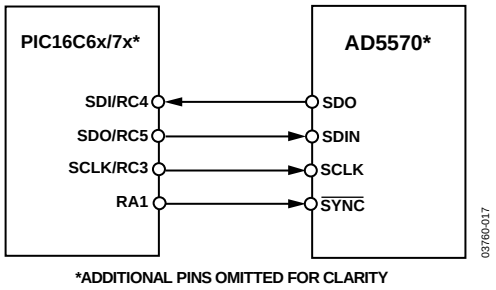

Figure 45. AD5570 to PIC16C6x/7x Interface

EVALUATION BOARD

The AD5570 comes with a full evaluation board to aid designers in evaluating the high performance of the part with minimal effort. The evaluation board requires a power supply, a PC, and an oscilloscope.

The AD5570 evaluation kit includes a populated, tested AD5570 printed circuit board. The evaluation board interfaces to the parallel interface of the PC. Software is available with the evaluation board, which allows the user to easily program the AD5570. A schematic of the evaluation board is shown in Figure 46. The software runs on any PC that has Microsoft Windows® 95/98/ME/2000 installed.

An application note containing full details on operating the evaluation board is available.

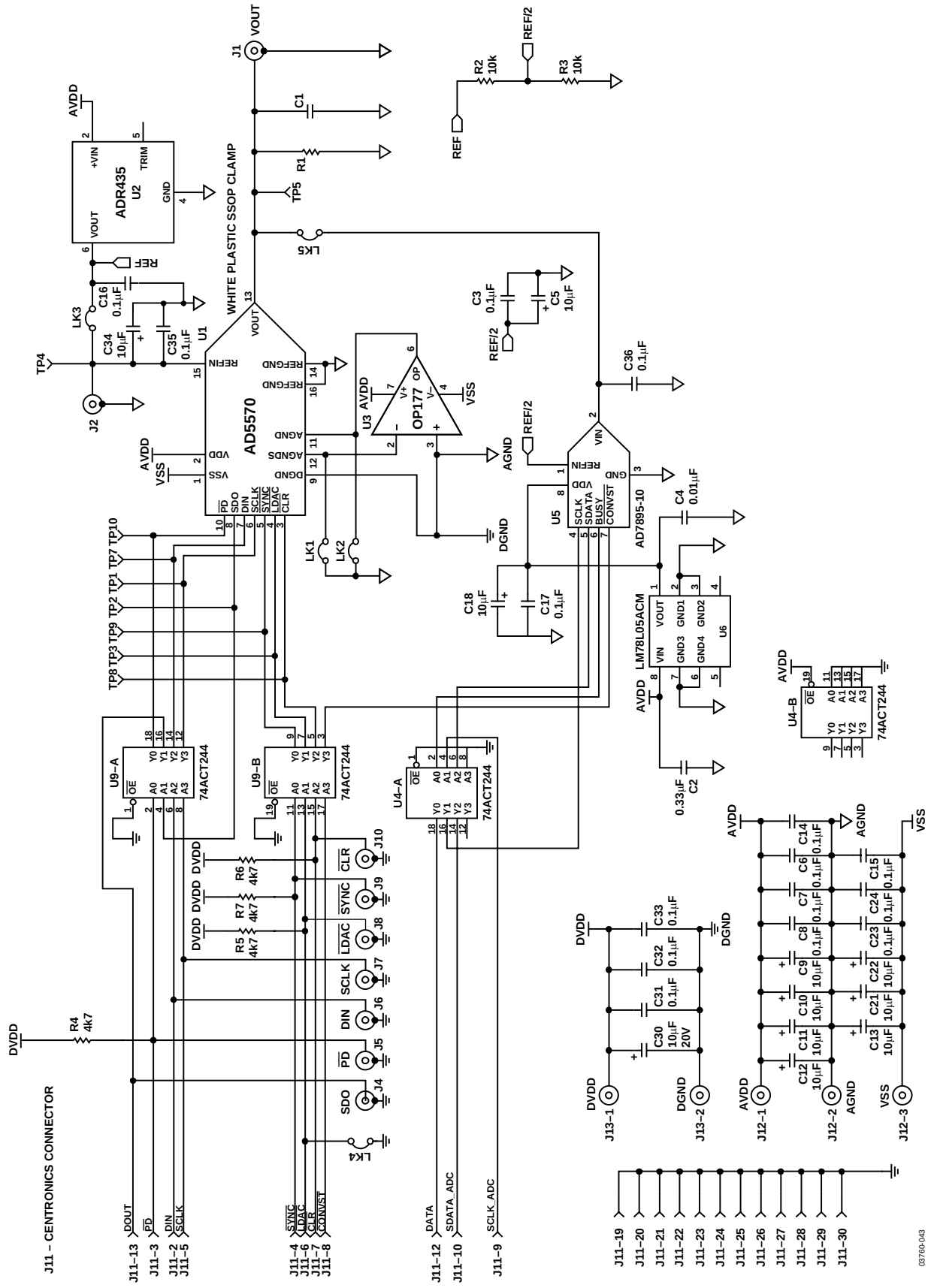

Figure 46. Evaluation Board Schematic

OUTLINE DIMENSIONS

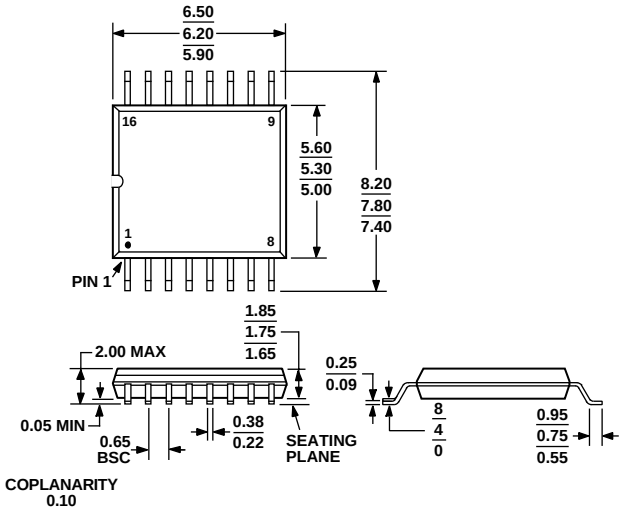

Figure 47. 16-Lead Shrink Small Outline Package [SSOP]
(RS-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5570ARS	−40° C to +85° C	16-Lead SSOP	RS-16
AD5570ARS-REEL	−40° C to +85° C	16-Lead SSOP	RS-16
AD5570ARS-REEL7	−40° C to +85° C	16-Lead SSOP	RS-16
AD5570BRS	−40° C to +85° C	16-Lead SSOP	RS-16
AD5570BRS-REEL	−40° C to +85° C	16-Lead SSOP	RS-16
AD5570BRS-REEL7	−40° C to +85° C	16-Lead SSOP	RS-16
AD5570WRS	−40° C to +125° C	16-Lead SSOP	RS-16
AD5570WRS-REEL	−40° C to +125° C	16-Lead SSOP	RS-16
AD5570WRS-REEL7	−40° C to +125° C	16-Lead SSOP	RS-16
AD5570YRS	−40° C to +125° C	16-Lead SSOP	RS-16
AD5570YRS-REEL	−40° C to +125° C	16-Lead SSOP	RS-16
AD5570YRS-REEL7	−40° C to +125° C	16-Lead SSOP	RS-16
EVAL-AD5570EB		Evaluation Board	

C03760–0–4/05(A)